REMARKS

By the above actions, claims 1-3 and 16-17 have been amended. Additionally, six replacement sheets of drawings are appended to this Amendment. In view of these actions and the following remarks, further consideration of this application is requested.

With regard to the objection to the drawings, the appended replacement sheets of drawings add descriptive labels to Figs. 1-3, 6a, 6b, and 7. As a result, this objection should now be withdrawn.

Likewise, claim 3 was objected to for failing to identify the scaling unit as being the "analog" scaling unit. This deficiency has been corrected above, so that this rejection should now be withdrawn.

Claims 2-6, 10 and 17 have been rejected for indefiniteness under 35 U.S.C. § 112. To the extent that this rejection of claims 2-6 & 10 is based upon language of claim 2 that has been deleted above, this rejection should now be withdrawn. Furthermore, claim 17 has been conformed with claim 3, the problematic reference to the active integrator being deleted, so that this rejection should be withdrawn relative to claim 17 as well.

Claim 16 has been rejected under 35 U.S.C. § 102 as being anticipated by the patent to Haynes. However, since this claim has been amended to conform with claim 1, with respect to which the rejection based on Haynes was withdrawn, the rejection of claim 16 should be withdrawn for the same reasons as resulted in the withdrawn of this rejection relative to claim 1.

Claims 1, 2, 9, & 16 have rejected under 35 U.S.C. § 102 as being anticipated by the patent to Roper et al., while claims 11-13 have been rejected under 35 U.S.C. § 103 as being unpatentable over the combination of the patents to Roper et al. and Haynes, while the remaining claims have been rejected under 35 U.S.C. § 103 based on the Roper et al. patent when viewed in combination with various other references. All of these rejections appear to be based on upon a misunderstanding of the Roper et al., particularly with respect to the nature of the connection between the processor circuit and the sensor, and regarding the shifting of the analog end stage and processor circuit into a sleep mode.

While both the invention and Roper et al. relate to an electrical transducer using a two-wire process, with an analog sensor, an analog end stage which is connected downstream

of the sensor and a processor circuit. Furthermore, even though the object of the present invention and the object solved by Roper are very similar, as will be apparent form the following, the solution disclosed by Roper is totally different from the solution of the present invention.

In electrical transducers using the two-wire process, there exists the problem that, in the least favorable case, only 4 mA – or less – is available as a power supply to all electronic components. It follows that conventional, economical microprocessors can be operated only with a short cycle time in order to achieve the required low power consumption of the microprocessor. However, this results in that only relatively slow changes of the quantity to be measured can be detected with such an electrical transducer. Therefore, modern electrical transducers face the conflict between the requirements for processing speed (which means high power consumption) on the one hand, and the power supply of the circuit components, on the other hand. This conflict is discussed in paragraph [0005] of the present application, and that an object of the invention is, thus, to provide an electrical transducer, which solves the above-mentioned conflict; which has low power consumption and still ensures high response speed is noted in paragraph [0007] of the present application.

To reduce the power consumption of the processor circuit, which generally has a microprocessor, in the electrical transducer of the invention, in normal operation, the processor circuit of the transducer is temporarily shifted into the sleep mode. Due to the described measure of shifting the processor circuit in normal operation of the transducer temporarily into the sleep mode, the power consumption of the processor circuit can be reduced to the required value, but this measure leads, at the same time, to the fact that the analog/digital converter connected upstream of the processor circuit or the downstream digital/analog converter cannot be active when the processor circuit is in the sleep mode. In the transmission path of sensor, analog/digital converter, microprocessor, digital/analog converter, analog end stage, this would lead to the electrical transducer not being able to follow the change in the quantity which is to be measured with the desired response speed.

Therefore, in accordance with the present invention, **an analog scaling unit is inserted in the analog measurement signal transmission path**, to which unit the output signal of the sensor and the at least one analog setting value are supplied as noted in paragraph [0008]. This results in the output signal of the sensor being routed not only past the

processor circuit, specifically via the analog measurement signal transmission path, but scaling of the electrical transducer by the analog scaling unit is possible. Applying an analog adjustment value to the analog scaling unit ensures that the analog adjustment value remains unchanged even during the sleep mode of the processor circuit.

Roper et al. disclose a two-wire industrial process control transmitter, which comprises a sensor 14, including a sensor charge circuit 18 and a sensor detector circuit 16, a A/D converter 20, 42, a microprocessor 22, 50 and an analog end stage 28, 56 (I/O-circuit). However, contrary to the Examiner's assertion in the Office Action on page 5, the processor circuit (microprocessor 22, 50) is connected serially between the sensor 14 and the analog end stage 28, 56. It appears that the Examiner has compared the sensor detector circuit 16, shown in Fig. 2 of Roper et al. with the analog end stage, mentioned in claim 1 of the present patent application, which is not correct. From Figs. 1 &. 2 of this reference, it should be clear that, in the electrical transducer disclosed by Roper et al., the sensor detector circuit 16, as well as the sensor charge circuit 18, form part of the sensor 14, whereas the analog end stage of this transducer is realized by the input/output circuit 28, 56.

That is, these figures show that the processor circuit (microprocessor 22, 50) is **connected serially** between the sensor and the analog end stage (input/output circuit 28, 56). Therefore, an analog measurement signal transmission path, as set forth in claim 1, is does **not** exist.

On page 5 of the Office Action it is said, that during normal operation of the electrical transducer, the processor circuit is shifted temporarily into a law-power sleep mode (abstract and column 3, lines 23-30). However, in column 3, lines 23 to 30 of Roper et al., that have been cited by the Examiner, it is stated that:

> In some embodiments of the invention, the analog measurement circuit is operated at a high voltage and the digital circuit is operated at a low voltage, with the high voltage being selected so that the power consumed by the analog measurement circuit is no more than 18 mW minus the power consumed by the digital circuit and the current drawn by the analog measurement circuit is no more than 3 mA minus the current drawn by the digital circuit.

In contrast to what is said by the Examiner, Roper et al. **does not** disclose an electrical transducer, wherein, during normal operation, the processor circuit is shifted temporarily into a low-power sleep mode.

What is disclosed by Roper et al. is a transducer, wherein the analog and digital elements of the transducer are separated into an analog IC chip 70 and a digital IC chip 72. Additionally, the operating power for the digital system circuit is decreased whereas the operating power for the analog measurement circuit is increased, which results in increased resolution. This can be seen from the statement in column 2, lines 48 to 55, that:

> In accordance with the present invention, the analog and digital portions of the analog-to-digital converter are supported by separate dies .... The operating power for the digital system circuit is decreased, and the power savings may be applied to the analog measurement circuit to increase resolution, and hence rangeability of the transmitter.

This principal of increasing the current of the analog measurement circuit, because of the reduced power consumption of the digital circuit, is described in greater detail in column 6, lines 21 to 43.

Additionally, because the microprocessor 50 is connected serially between the sensor and the analog end stage, and therefore, part of the measurement signal transmission path, if microprocessor 50 would be shifted temporarily into a sleep mode, this would reduce the processing speed and the resolution of the transducer. Therefore, there is no reason, motivation or suggestion in the Roper et al. reference to shift the microprocessor temporarily into a sleep mode, as described in claim 1.

Adding the teachings of Hayes to those of Roper et al. does not overcome the indicated deficiencies of Roper et al. relative to the presently claimed invention. As was mentioned in applicants' preceding response, and evidently recognized by the Examiner in by his withdrawal of the rejection of claim 1 previously made based on the Hayes patent, Hayes discloses a two-wire ultrasonic transmitter, which comprises a transducer, a drive circuit, an amplifier circuit, a detector circuit, a control circuit and a processor circuit, which is connected serially between the transducer and the end stage. In order to reduce the power consumption of this transmitter, the transmitter is shifted temporarily into a sleep mode.

However, because neither Roper nor Haynes disclose an analog measurement signal transmission path as set forth in claim 1, there is no motivation or suggestion to combine these two references in a manner which would result in an electrical transducer comprising an analog measurement signal transmission path including an analog scaling unit as claimed.

As for the other references relied upon by the Examiner with regard to incidental features of various dependent claims, none of these references can in anyway address the basic shortcomings of the Roper et al. and Haynes patents. Thus, the rejections based on these other references should be withdrawn along with those which rely solely on the Roper et al. patent and/or the Haynes patent.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with applicant's representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Respectfully submitted,

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